APPENDIX E

RADAR SIMULATION

INTRODUCTION

This appendix discusses the techniques used to simulate the primary radar performance so that trade-off investigations could be made as a function of radar signal processing characteristics in the presence of a parametric range of noise, desired signal, and asynchronous interfering signal conditions. The primary radar simulated was the ASR-7. Only the normal and Moving Target Indicator (MTI) channels of the radar were simulated. The portion of the ASR-7 radar simulated was the processor unit (i.e., normal channel envelope detector output and MTI channel phase detector output to the radar output).

In addition, for study of the properties of the feedback enhancer, the simulation provides the capability to use a feedback enhancer in place of the ASR-7 binary enhancer. It should be noted however, that the ASR-7 does not have a feedback enhancer.

PROCESSOR UNIT DESCRIPTION

A detailed description of the primary radar processor unit is given in Section 3. Figure E-1 shows a block diagram of the ASR-7 processor unit hardware which was simulated. The portion of the processor unit normal channel simulated was the normal channel enhancer functional switch, enhancer and alignment hardware. The portion of the processor unit MTI channel simulated was the MTI cancellers, enhancer functional switch, enhancer, and alignment hardware. The simulation model has the capability of displaying the processor unit output in the unenhanced and enhanced modes of both the normal and MTI channels on either an oscilloscope or Plan Position Indicator (PPI) display.

In order to reduce the simulation model computer run time and for analytical simplicity, the conventional analog-to-digital (A/D) and digital-to-analog (D/A) converters at the processor unit input and output respectively were not simulated. However, the received signal amplitudes were simulated in time by dividing the radar receive period after each transmitted pulse into 1200 range bins .625 microseconds long corresponding to the actual A/D and D/A converter hardware of the ASR-7. Since the quantization noise caused by A/D converters is small compared to the inherent receiver noise, not simulating the A/D and D/A converters will not result in unrealistic simulation of the ASR-7 processor unit.

The clock timing for the range bins and desired signal characteristics are shown in Figure E-2. The ASR-7 system clock timing and desired signal

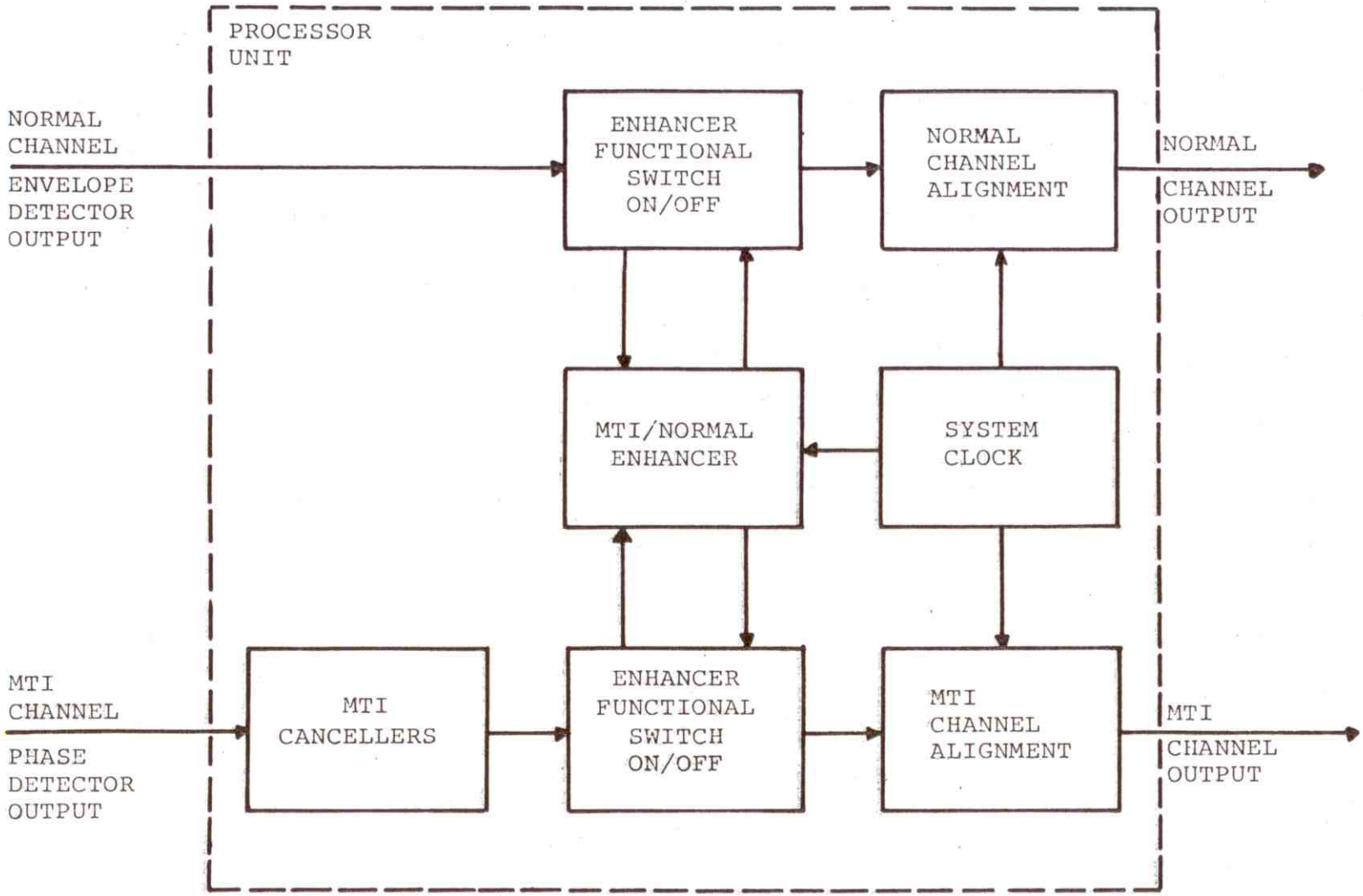

Figure E-1. Block Diagram of Simulated ASR-7 Processor Unit

PW = 0.833 μsec

PRF = 1002 Average (6-Pulse Stagger)

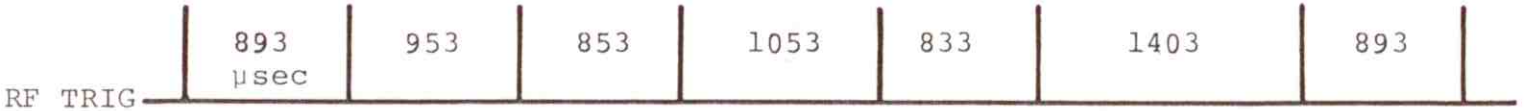

Figure E-2. Clock Timing and Desired Signal Characteristics for ASR-7 Radar

characteristics were simulated for the radar operating in the six-stagger mode which has an average Pulse-Repetition-Frequency (PRF) of 1002 Pulses-Per-Second (PPS). The clock timing also controls the video realignment (destaggering to an average PRF of 1002) at the processor output for Plan Position Indicator (PPI) display. Using the nominal ASR-7 characteristics, the degrees of antenna scan per pulse (ϕ_S) is given by:

$$\phi_S = \frac{6 \cdot RPM}{PRF} = \frac{6 \cdot 12}{1002} = 0.0718562874°/pulse \qquad \text{(E-1)}$$

where:

RPM = Antenna scan rate, in rpm (12 for ASR-7)

PRF = Radar pulse repetition frequency, in PPS (1002 for ASR-7)

The number of Azimuth Change Pulses (ACP) per antenna scan for the ASR-7 is:

$$ACP = \frac{360°}{\phi_S} = 5010 \qquad \text{(E-2)}$$

Therefore, in summary the simulation of the ASR-7 processor unit was done by:

a. Dividing the receive period after each pulse into 1200 range bins .625 microseconds long,

b. each range bin is approximately 0.0718 degrees wide, and

c. there are 5010 azimuth change pulses (ACPs) per antenna scan.

DESIRED SIGNAL

Figure E-2 shows the pulse width and PRF stagger sequence of the ASR-7 desired signal. The radar simulation model has the capability of simulating a single desired target at any specified range and bearing. The received desired signal pulse train (number of pulses from a target (N)) consists of 20 pulses determined by:

$$N = \frac{PRF \cdot BW}{6 \cdot RPM} = \frac{(1002)(1.5)}{(6)(12)} \simeq 20 \qquad \text{(E-3)}$$

where:

PRF = Radar pulse repetition frequency, in PPS (1002 for ASR-7)

BW = Antenna 3 dB beamwidth, in degrees (1.5 degrees for ASR-7)

RPM = Antenna scan rate, in rpm (12 for ASR-7)

The range bin in which the target is located (TRB) was calculated by:

$$TRB = \frac{TR}{RTT \cdot RBT} \qquad \text{(E-4)}$$

where:

TRB = Target range bin location, between 1 and 1200

TR = Target range, in nautical miles

RTT = Round-trip time, equals .081 nautical miles per microsecond

RBT = Range bin time, equals .625 microseconds per range bin

The target location (bearing) in Azimuth Change Pulses (ACP) was calculated by:

$$TACP = \frac{TB \cdot PRF}{6 \cdot RPM} \qquad \text{(E-5)}$$

where:

TACP = Target azimuth change pulse, between 1 and 5010

TB = Target bearing, in degrees

PRF = Radar pulse repetition frequency, in PPS (1002 for ASR-7)

RPM = Antenna scan rate, in rpm (12 for ASR-7)

The desired signal voltage amplitude in each range bin as a function of the desired signal signal-to-noise ratio (S/N) is discussed later in the normal and MTI channel simulation sections.

INTERFERING SIGNALS

Three types of interfering radar signals were simulated: ASR-5, ASR-8, and AN/FPS-90. The radar simulation model has the capability of having any combination of the three interfering sources present. Figures E-3 through E-5 show the signal timing characteristics of the ASR-5, ASR-8, and AN/FPS-90 interfering radars used in the simulation model. The interfering signal voltage amplitude in each range bin as a function of the interference-to-noise ratio (I/N) is discussed later in the normal and MTI channel simulation sections.

NOISE

In range bins where there was no desired signal or interfering signal the radar inherent noise level was simulated. The simulation of the noise amplitude in each range bin is discussed in the normal and MTI channel simulation sections.

NORMAL CHANNEL SIMULATION

The following is a discussion of the techniques used to simulate the noise, desired signal, and interfering signal levels in the normal channel, and the processor unit hardware in the normal channel.

Noise Distribution

The voltage amplitude distribution of the noise at the normal channel envelope detector output is Rayleigh distributed. The Rayleigh distributed voltage amplitude characteristics of the noise were simulated by letting

$$n_{edo}(t) = \sigma\sqrt{-2 \ln U} \qquad \text{(E-6)}$$

where:

σ = RMS noise level at detector input, in volts

U = Random number uniformly distributed between 0 and 1.0

For each range bin in which noise only is present, a noise voltage amplitude using Equation E-6 was simulated by randomly selecting values between 0 and 1.0 for U.

Signal-Plus-Noise Distribution

The signal-plus-noise voltage amplitude distribution at the envelope detector output has a Rice distribution (also called the Marcum "Q" function). The amplitude characteristics of the signal-plus-noise for the

PW = 0.833 μsec
PRF = 1170 Average (2-Pulse Stagger)

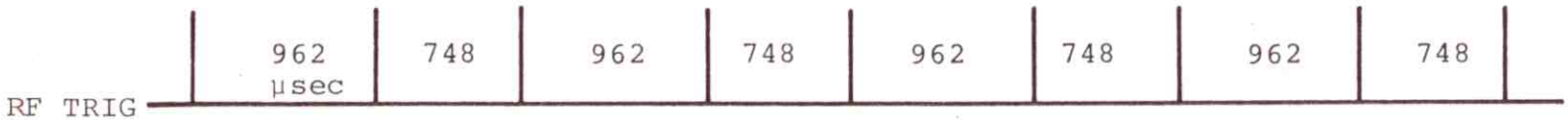

Figure E-3. ASR-5 Interfering Signal Characteristics

PW = 0.6 μsec
PRF = 1040 Average (4-Pulse Stagger)

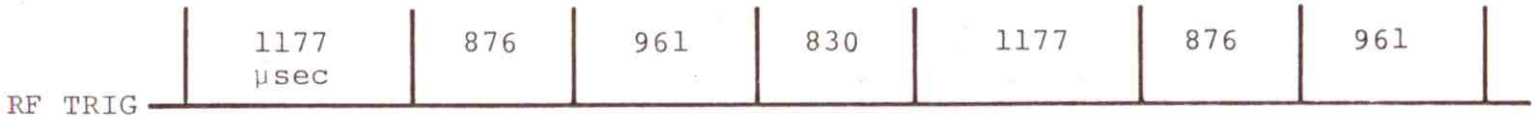

Figure E-4. ASR-8 Interfering Signal Characteristics

PW = 2.0 μsec
PRF = 370 Pulses

Figure E-5. AN/FPS-90 Interfering Signal Characteristics

desired and interfering signals were simulated by:

$$(S+N)_{edo}(t) = \sqrt{X^2+Y^2} \qquad \text{(E-7)}$$

where:

$X = R \cos(2\pi V) + A$

$Y = R \sin(2\pi V)$

$R = \sigma\sqrt{-2 \ln U}$

σ = RMS noise level at envelope detector input, in volts

A = Peak-signal level at envelope detector input, in volts

U and V = Random numbers between 0 and 1.0

For the case where "A" equals zero (no signal present), Equation E-7 is equivalent to Equation E-6. Equation E-7 was used to simulate the signal-plus-noise voltage amplitude for both the desired pulse train and interfering signal. The timing of the desired and undesired signals were programmed using List Processing Techniques. For each range bin in which a desired or interfering pulse is present, a signal-plus-noise voltage amplitude using Equation E-7 was simulated by randomly selecting values between 0 and 1.0 for U and V. Figure E-6 shows the simulated signal-plus-noise voltage amplitude distribution as a function of the signal-to-noise ratio (S/N) in dB generated using Equation E-7. The RMS noise voltage level (σ) was set at .25 volts. This corresponds to a one volt peak noise level generally set at the radar receiver output.

Normal Channel Enhancer

The ASR-7 enhancer hardware which was simulated is shown in Figure E-7. The enhancer is basically a digital circuit with an adjustable threshold detector as a simple A/D converter. The enhancer circuit consists of the threshold detector, the digital adder/subtracter circuits, a full range shift register storage, and a D/A converter. If an echo signal exceeding the set threshold level exists in any given range bin, the enhancer stores a one level digital signal in its shift register memory. If the signal continues above the threshold in the given range bin, the enhancer will increase the level stored in each PRF period until a maximum amplitude of 31 is reached. If in any PRF period the signal fails to exceed the threshold level, the enhancer subtracts from the stored level in that particular range bin. The clock timing for the shift register was simulated for the ASR-7 six-stagger mode (see Figure E-2).

A detailed discussion of the signal processing properties of the ASR-7 enhancer is given in Appendix D.

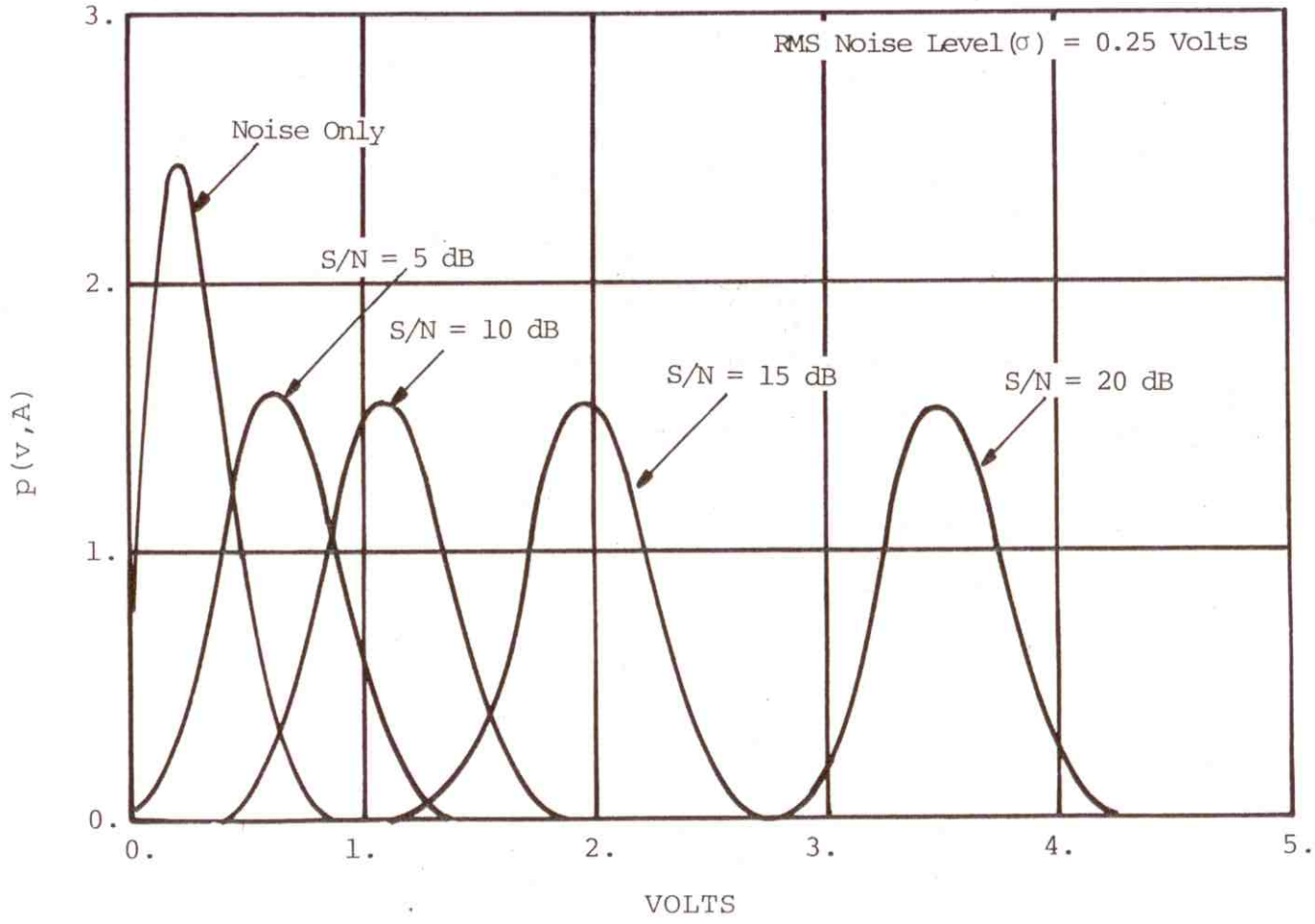

Figure E-6. Probability Density Function for Noise Only and for Signal-Plus-Noise at the Normal Channel Envelope Detector Output.

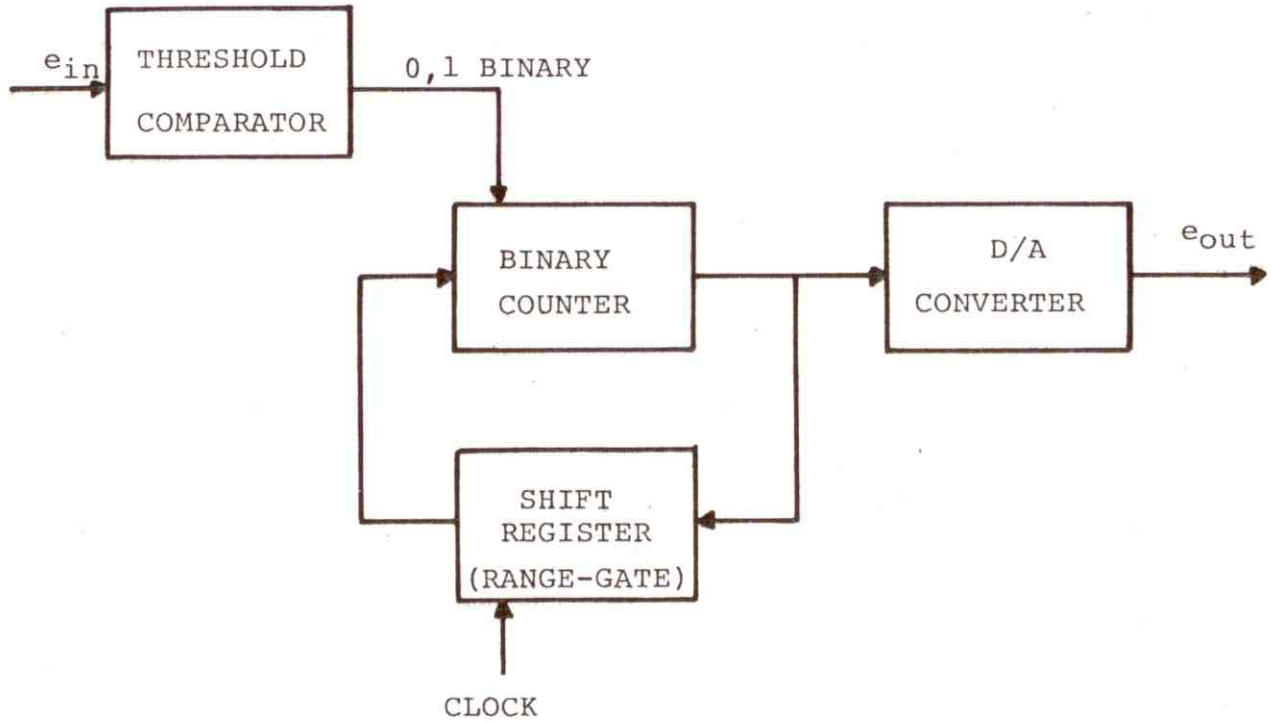

Figure E-7. ASR-7 (AN/GPN-12) Binary Integrator Block Diagram

Normal Channel Alignment

The normal channel alignment circuits provide the delay required during STAGGER PRF operation to insure that a specific range bin in each PRF receive period occurs at the average PRF of 1002. The STAGGER PRF operation and clock timing which was simulated is shown in Figure E-2. The stagger video occurs with the PRF periods of 893 microseconds, 953 microseconds, 853 microseconds, 1053 microseconds, 833 microseconds, and 1403 microseconds. To align these with the average period of 998 microseconds, clock timing from the RF trigger is used to control the alignment circuit delay selection.

MTI CHANNEL SIMULATION

The following is a discussion of the techniques used to simulate the noise, desired signal, and interfering signal in the MTI channel, and the processor unit hardware in the MTI channel.

Noise Distribution

The voltage amplitude distribution of the noise at the phase detector output is Gaussian distributed. The Gaussian distributed voltage amplitude characteristics of the noise were simulated by letting:

$$n_{pdo}(t) = R \cos 2\pi V \qquad \text{(E-8)}$$

where:

$R = \sigma\sqrt{-2 \ln U}$

σ = RMS noise level at phase detector input, in volts

U and V = Random numbers uniformly distributed between 0 and 1.0

For each range bin in which noise only is present, a noise voltage amplitude using Equation E-8 was simulated by randomly selecting values between 0 and 1.0 for U and V.

Signal-Plus-Noise Distribution

The signal-plus-noise voltage amplitude distribution at the phase detector output was simulated by:

$$(S+N)_{pdo}(t) = R \text{ Cos } 2\pi V + A \cos 2\pi W \qquad \text{(E-9)}$$

where:

A = Peak-signal level at phase detector input, in volts

V and W = Random numbers uniformly distributed between 0 and 1.0

For the case where "A" equals zero (no signal present), Equation E-9 is equivalent to Equation E-8. Equation E-9 was used to simulate the signal-plus-noise voltage amplitude for both the desired pulse train and interfering signal. The timing of the desired and undesired signals were programmed using List Processing Techniques. For each range bin in which a desired or interfering pulse is present, a signal-plus-noise voltage amplitude using Equation E-9 was simulated by randomly selecting values between 0 and 1.0 for U, V, and W. Figure E-8 shows the simulated signal-plus-noise voltage amplitude distribution as a function of the signal-to-noise ratio (S/N) in dB generated using Equation E-9. The rms noise voltage level was set at .25 volts.

MTI Cancellers

The MTI double stage canceller hardware in the ASR-7 radar was simulated. It was necessary to simulate the ASR-7 MTI canceller hardware in order to investigate the performance of the ASR-7 enhancer in the presence of asynchronous interference since the impulse response of a double stage MTI canceller with feedback will produce several synchronous pulses. A detailed discussion of the signal transfer properties of a double stage MTI canceller to asynchronous interference is discussed in Appendix C. The following is a discussion of the simulation of the ASR-7 double stage MTI canceller.

The ASR-7 digital canceller consists of two identical delay line type cancellers in cascade, with switch selectable feedback. Figure E-9 shows the canonical form of the ASR-7 MTI canceller which was simulated. The figure shows the transfer function coefficients which represent the ASR-7 hardware. The feedforward coefficients (a_i) are $a_o = 1/2$, $a_1 = -1$, and $a_2 = 1/2$. The feedback coefficients (b_i) for the various canceller modes are:

CANC 2 :	$b_1 = 0$;	$b_2 = 0$
25 dB SCV:	$b_1 = 1\frac{1}{4}$;	$b_2 = -\frac{1}{2}$
30 dB SCV:	$b_1 = 1$;	$b_2 = -\frac{1}{2}$
35 dB SCV:	$b_1 = \frac{3}{4}$;	$b_2 = -\frac{1}{2}$
40 dB SCV:	$b_1 = \frac{1}{2}$;	$b_2 = -\frac{1}{2}$

A digital word from each range bin is fed into the canceller. If this range bin contains only clutter, the canceller output will be virtually zero. If it contains a moving target the difference amplitude will represent a sample taken from the doppler cycle. The storage element in each canceller consists of eight parallel shift register chains 1200 range bins long. The digital words are clocked in parallel down the 1200 shift-register bins at a 1.6 MHz rate. The timing for the delays in the MTI canceller were simulated for the ASR-7 six-stagger mode shown in Figure E-2. List Processing Techniques were

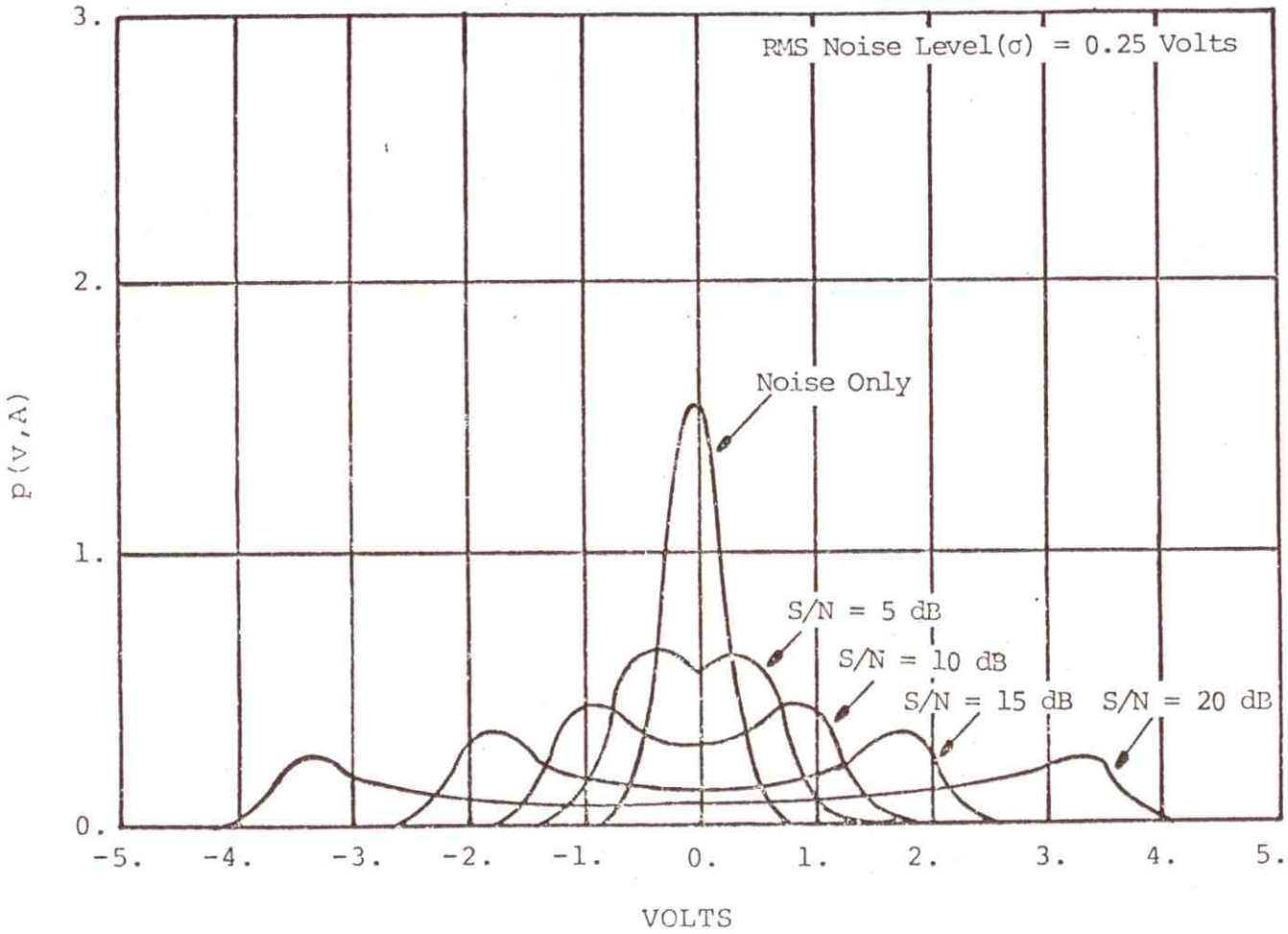

Figure E-8. Probability Density Function for Noise Only and for Signal-Plus-Noise at the MTI Phase Detector Output.

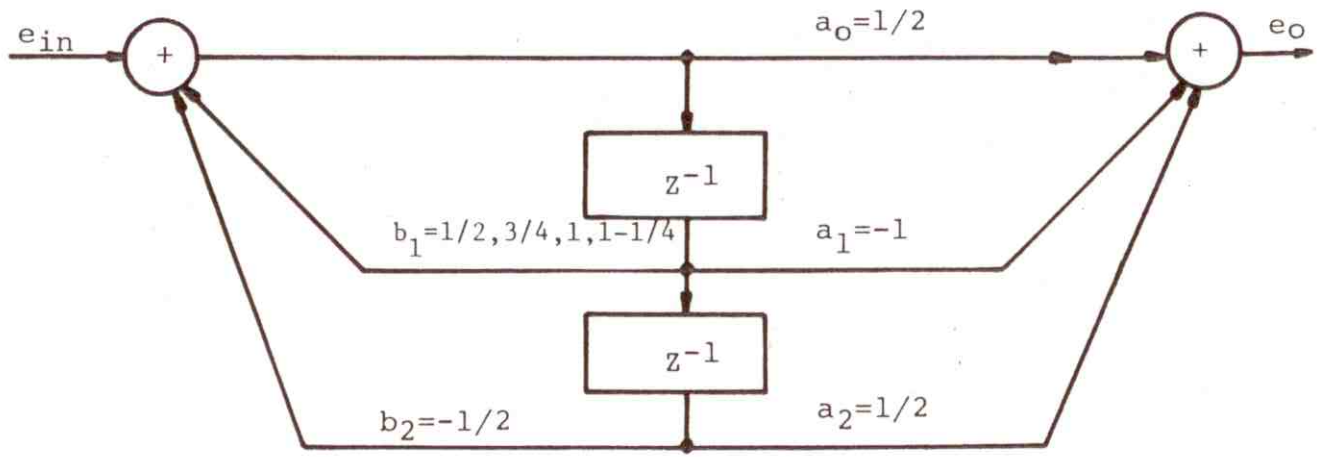

Figure E-9. Canonical Form of Simulated ASR-7 MTI Canceller

used in programming the timing of the ASR-7 six-stagger sequence.

Appendix C contains a detailed discussion of the signal processing properties of the MTI cancellers.

MTI Channel Enhancer

The MTI channel enhancer circuitry is identical to the normal channel enhancer. The simulation of the enhancer was discussed in the normal channel simulation section.

MTI Channel Alignment

The MTI channel alignment circuitry is identical to the normal channel alignment circuitry. The simulation of the alignment circuitry was discussed in the normal channel simulation section.

FEEDBACK ENHANCER

As mentioned at the beginning of this appendix, a feedback enhancer capability was added to the simulation. Figure E-10 shows the feedback enhancer model used in the simulation. The first three blocks: the attenuator, subtractor and bottom clipper are ,strictly speaking, not part of the ASR-8 enhancer circuit board (which it attempts to model). However, these functions are effectively found in other circuits, and it was found necessary to include them to achieve realistic results. Appendix D has a detailed discussion of the feedback integrator.

OUTPUT DISPLAY

Two radar output displays were simulated: the radar output oscilloscope display, and the radar output PPI display. The radar simulation model has the capability of displaying both the normal and MTI channels in the unenhanced and enhanced modes. Appendix D contains oscilloscope display outputs as a function of a parametric range of noise, desired signal, and asynchronous interfering conditions. Also, the trade-offs of the desired signal properties in utilizing an enhancer to suppress interfering signals are discussed in Appendix D. Figure E-11 is 45 degrees of a simulated PPI display of interference.

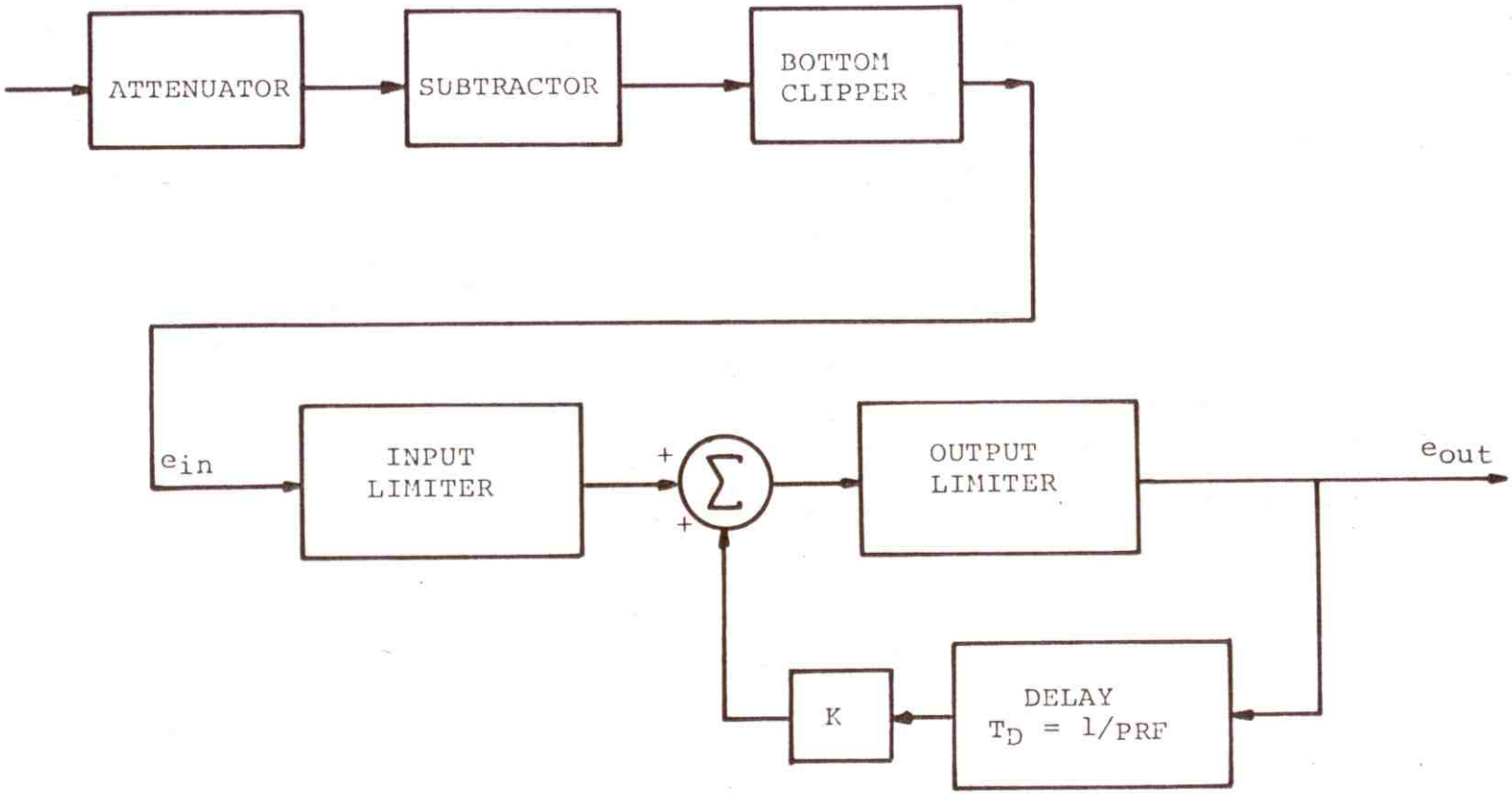

Figure E-10. Feedback Integrator Block Diagram

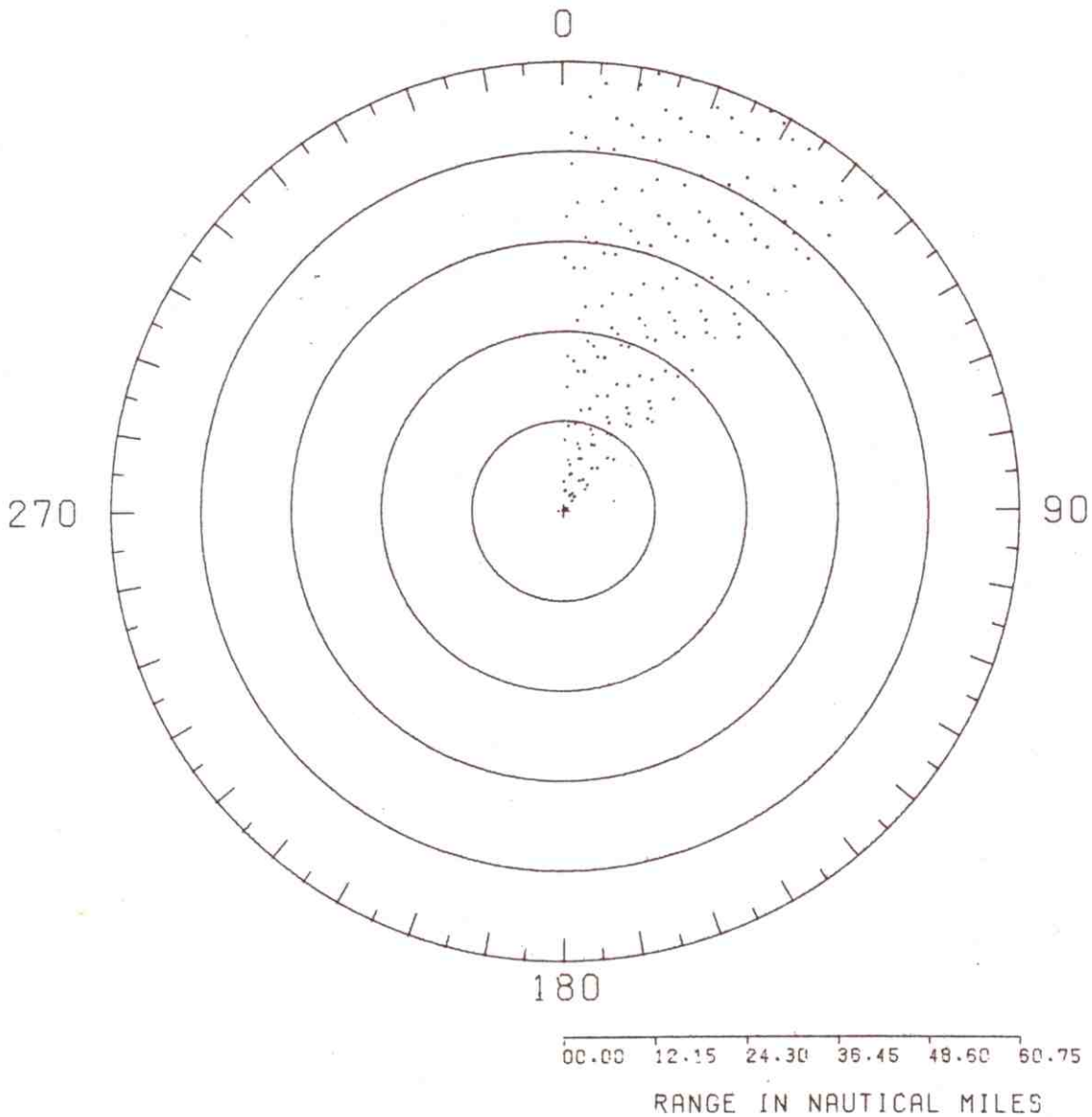

Figure E-11. Simulated PPI Display of Interference